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2308  
DATE MAILED:

02/14/94

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

ART UNIT PAPER NUMBER

5

This application has been examined  Responsive to communication filed on \_\_\_\_\_  This action is made final.

A shortened statutory period for response to this action is set to expire Three month(s), No days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

**Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:**

1.  Notice of References Cited by Examiner, PTO-892. 2.  Notice re Patent Drawing, PTO-948.  
3.  Notice of Art Cited by Applicant, PTO-1449. 4.  Notice of Informal Patent Application, Form PTO-152.  
5.  Information on How to Effect Drawing Changes, PTO-1474. 6.  \_\_\_\_\_

**Part II SUMMARY OF ACTION**

1.  Claims 1-10 are pending in the application.

Of the above, claims \_\_\_\_\_ are withdrawn from consideration.

2.  Claims \_\_\_\_\_ have been cancelled.

3.  Claims \_\_\_\_\_ are allowed.

4.  Claims 1-10 are rejected.

5.  Claims \_\_\_\_\_ are objected to.

6.  Claims \_\_\_\_\_ are subject to restriction or election requirement.

7.  This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8.  Formal drawings are required in response to this Office action.

9.  The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are  acceptable.  not acceptable (see explanation or Notice re Patent Drawing, PTO-948).

10.  The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_ has (have) been  approved by the examiner.  disapproved by the examiner (see explanation).

11.  The proposed drawing correction, filed on \_\_\_\_\_, has been  approved.  disapproved (see explanation).

12.  Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has  been received  not been received  been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_

13.  Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14.  Other

**EXAMINER'S ACTION**

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1. The drawings are objected to because the labels in figures 1, 2a-2d and 3 are not clear, delete "Figure 1" and insert -- Fig. 1 -- and figures 2a-2d and 3-7, "Fig" should be "Fig.". Correction is required.

2. The specification is replete with grammatical errors too numerous to mention specifically. The specification should be revised carefully. Examples of such errors are: Page 4, line 14, delete "Figure 2, including figures 2a-2d, is a waveform" and insert -- Figures 2a-2d are waveform". Page 4, line 15, delete "diagram" and insert -- diagrams --. Page 13, line 16, delete Figure 2 and insert -- Figures 2a-2d --.

3. Claims 1-7 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 6 and 7, the phrase logic control means responsive to data access activity" fails to recite the responsibility of the logic control means toward data access activity.

Line 10, the word "sufficient" is general and not define.

Claim 3, line 3, the phrase "a switching regulator" fails to recite a type of the regulator.

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4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Watanabe, U.S. Pat. No. 4964073.

Watanabe discloses supplying variable voltage (abstract, lines 1-6 and figure 3, devices 14 and 15) and generating address and control signals (figure 3, devices 19 and 20) and controlling said power control means to supply voltage to said memory (figure 3 and abstract).

Therefore, Watanabe discloses all of the items as claimed.

5. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same

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person or subject to an obligation of assignment to the same person.

Claims 2, 6 and 9 are rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe, U.S. Pat. No. 4964073 in view of Tuma et al, U.S. Pat. No. 5070474.

As per claim 2, Watanabe does not teach converting serial signals to parallel signals and performing error correction. Tuma teaches converting serial signals to parallel signals (figure 2, device 102) and performing error correction (figure 2, device 103). It would have been obvious to one of ordinary skill in the art to combine Watanabe and Tuma references to provide a system such as Watanabe's with a memory output signals conversion and error correction systems to improve the signals outputted from the memory because Tuma teaches that the signals that are outputted from a memory such as Watanabe's can be improved by conversion and filtering.

As per claim 6, Watanabe does not teach generating said address signals. Tuma teaches generating said address signals (figure 2, device 109 and 106). It would have been obvious to one of ordinary skill in the art to provide address signals to a memory in a system such as Watanabe's to improve the time needed to seek these signals because Tuma teaches generating the address signals to improve the seek time.

As per claim 9, Watanabe does not teach enabling communication with another dynamics power management device. Tuma

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teaches enabling communication with another dynamic power management device (figure 2, device 100). It would have been obvious to one of ordinary skill in the art to provide a system such as Watanabe's with an information exchange system because Tuma teaches exchanging information such as read and write with another system such as Watanabe's to improve communication between the systems.

6. Claims 3 and 4 are rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe, U.S. Pat. No. 4964073 in view of Nanno et al, U.S. Pat. No. 5239495.

As per claim 3, Watanabe does not teach means for selecting between alternate power sources and feeding voltage information back to said logic control means. Nanno teaches selecting between alternate power sources (column 14, lines 49 and 50) and feeding voltage information back to said logic control means (figure 1, devices 30 and 11). It would have been obvious to one of ordinary skill in the art to provide a system such as Watanabe with a feedback system and means for selecting between alternate power sources to control the power supply in order to consume power because Tuma teaches controlling power by using a feedback system and selecting between two alternate sources.

As per claim 4, Watanabe teaches maintain a specified voltage output (figure 3, device 15).

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Watanabe does not teach select one of said alternate power sources. Nanno teaches select one of said alternate power sources (column 14, lines 49 and 50). It would have been obvious to one of ordinary skill in the art to replace a power source in a system such as Watanabe's with an alternate power sources and select one of these sources to supply voltage because Nanno teaches selecting one alternate power sources to control the power supply to a system such as Watanabe's.

7. Claims 5, 8 and 10 are rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe, U.S. Pat. No. 4964073 in view of Cole et al, U.S. Pat. No. 5241680.

As per claim 5, Watanabe does not teach DMA, data sequencer and time sequencer. Cole teaches DMA (abstract) and time and data sequencers (figure 3A, devices 56 and DMA controller). It would have been obvious to one of ordinary skill in the art to combine Cole and Watanabe systems to provide a system such as Watanabe's with a DMA to improve the storage capability because Cole teaches a DMA to provide a support and an access to a main storage device.

As per claims 8 and 10, Watanabe does not teach different levels of voltage during a standby, a memory refresh and a memory access and a sleep mode. Cole teaches different levels of voltage during a standby (figure 3A, device 60 and 63), a memory refresh

(abstract, lines 3 and 4), a memory access (column 5, lines 10-15) and a sleep mode (figure 3A, device 60). It would have been obvious to one of ordinary skill in the art to provide a system such as Watanabe's with different modes such as sleep mode and standby mode to improve power consumption because Cole teaches different level voltage for the computer modes such as the sleep mode and the standby mode to reduce the power consumption.

8. Claim 7 is rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe, U.S. Pat. NO. 4964073 in view of Little et al, U.S. Pat. No. 5237699.

Watanabe does not teach slew rate. Little teaches slew rate (column 11, lines 45-49). It would have been obvious to one of ordinary skill in the art to provide to a system such as Watanabe with a slew rate controller because Little discloses a slew rate controller to control the signals inputted to a memory such as Watanabe's memory.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Davis whose telephone number is (703) 305-9640.

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Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9605.

February 8, 1994

*George Davis*  
GEORGE B. DAVIS  
PATENT EXAMINER  
GROUP 2300